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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,128	03/25/2002	Chao-Hu Liang	NAUP0385USA	5968

27765 7590 05/11/2004

NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	10/063,128	LIANG ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 02 December 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See the Attachment*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

Attachment

Response to Arguments

Applicant's arguments filed December 02, 2003 have been fully considered but they are not persuasive.

Rejection Under 35 U.S.C. 112

Applicants appear to contend that the claimed term "comprises a plurality of particles" do not fail to correspond in scope with the present invention. Applicants state: "Although most of the contaminants, such as organic contaminants, particles, metallic contaminants, adhering to the semiconductor wafer 100 are removed, however, **it is impossible to remove all of the contaminants with the now existing semiconductor technique. Therefore, the surface of the semiconductor wafer comprises a plurality of particles** (lines 2-3), which cannot be removed by the wet etching process and the wet cleaning process".

However, the instant specification fails to support Applicants' conclusion: **Therefore, the surface of the semiconductor wafer comprises a plurality of particles.** Applicants should point out a portion of the specification explicitly discloses that contaminants particles exist after the thorough clean.

Contrary to the Applicant assertion, the term "Nucleation is thus effectively **inhibited** to further avoid grains growing by way of small and large particles on the surface of the semiconductor wafer during crystallization" means "the defects have been suppressed by forming the polysilicon gate electrode by two steps deposit" rather than by the present of contaminants on the surface, since contaminants are the root of the defects that the present inventors have tried so hard, various cleaning process, to eliminate.

Further, Applicants state: "although most of the contaminants, such as organic contaminants, particles, metallic contaminants, adhering to the semiconductor wafer 100 are removed by the wet etching process and the wet cleaning process, **it is impossible to remove all of the contaminants with the now existing semiconductor technique**. The surface of the semiconductor wafer thus comprises a plurality of particles".

Applicants appear to admit that the present of contaminants particles on the semiconductor substrate are inherent, since they are impossible to remove.

However, the instant specification, page 6 [0025], discloses: "After removing the photoresist layer 112 , a wet etching process is performed. Usually, a megasonic scrubbing process is first performed. By utilizing vibration of the megasonic scrubbing process, contaminants adhering to the semiconductor wafer 100 **are removed**. An ammonium hydrogen peroxide mixture (APM) solution having a high PH value, **is then used to remove** organic contaminants and particles by way of an oxidation reaction at a temperature ranging from 80 to 90 °C. Finally, a SC-2 cleaning process is performed. A hydrochloric acid hydrogen peroxide mixture (HPM) solution, having a low PH value and at a temperature ranging from 80 to 90 °C, forms soluble complex ions **so as to remove** metallic contaminants". This paragraph clearly contradicting the Applicants assertion that contaminant particles exist on the semiconductor substrate.

With respect to claim 17, Applicants state: "In claim 9, the term "the two-step silicon deposition process comprises a first step low temperature amorphous silicon (α-Si) deposition process to avoid formation of particles and defects by inhibiting nucleation during the formation

of the polysilicon layer, and a second step high temperature polysilicon deposition process." **means that the formation of the particles have been avoided by the formation of the amorphous silicon layer as possible**.

However, since the formation of the particles **have been avoided** then, the non-existent particles should not have any shape.

Clearly claim 17 contradicting claim 9, for claiming a shape, "needle like", of something that does not exist, e.g., have been avoided.

Regarding Fig. 14, there is no particles shown in the drawing.

All rejections under 35 U.S.C. 112 are therefore, maintained.

Rejection Under 35 U.S.C. 102

With respect to claim 1, Applicants fail to point out which limitations, if any, of claim 1 do not teach by Balasubramanian '004.

Applicants state: "In addition, Balasubramanian never teaches how to **utilize** a first step amorphous silicon deposition process to inhibit occurrences of needle-like contamination on the surface of the final formed polysilicon film". Note that "utilizing" have been deleted from claim 1.

However, Balasubramanian clearly teaches forming a polysilicon layer by two steps deposit, first amorphous silicon layer at low temperature then polysilicon layer at high temperature. Therefore, it is more probable than not the depositing process of Balasubramanian also suppressed the formation of the defects as claimed, e.g., inherent.

Therefore, there is no difference between the teaching of Balasubramanian and the limitation as claimed by claim 1, as well as claims 7 and 8.

With respect to claims 2-3 and 5-6, since claim 1 is anticipated by Balasubramanian, therefore, claims 2-3 and 5-6 are obvious over the teaching of Balasubramanian in view of Yu '167 and APA.

With respect to claims 9-12 and 14-17, Applicants allege that since claim 1 is not anticipated by Balasubramanian, and conclude that claim 9 is absolutely different from Balasubramanian, hence patentable.

However, as discussed above, Balasubramanian clearly anticipate claim 1 therefore, claim 9 is unpatentable over Yu and Balasubramanian, thus, claims 10-12, 14-17 and 4, 13 as well.

For those reasons, all the rejections are therefore, maintains.

LONG PHAM
PRIMARY EXAMINER